Intel Corporation
Silicon Technology Review

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SEMI – Strategic Business Conference
April 2003

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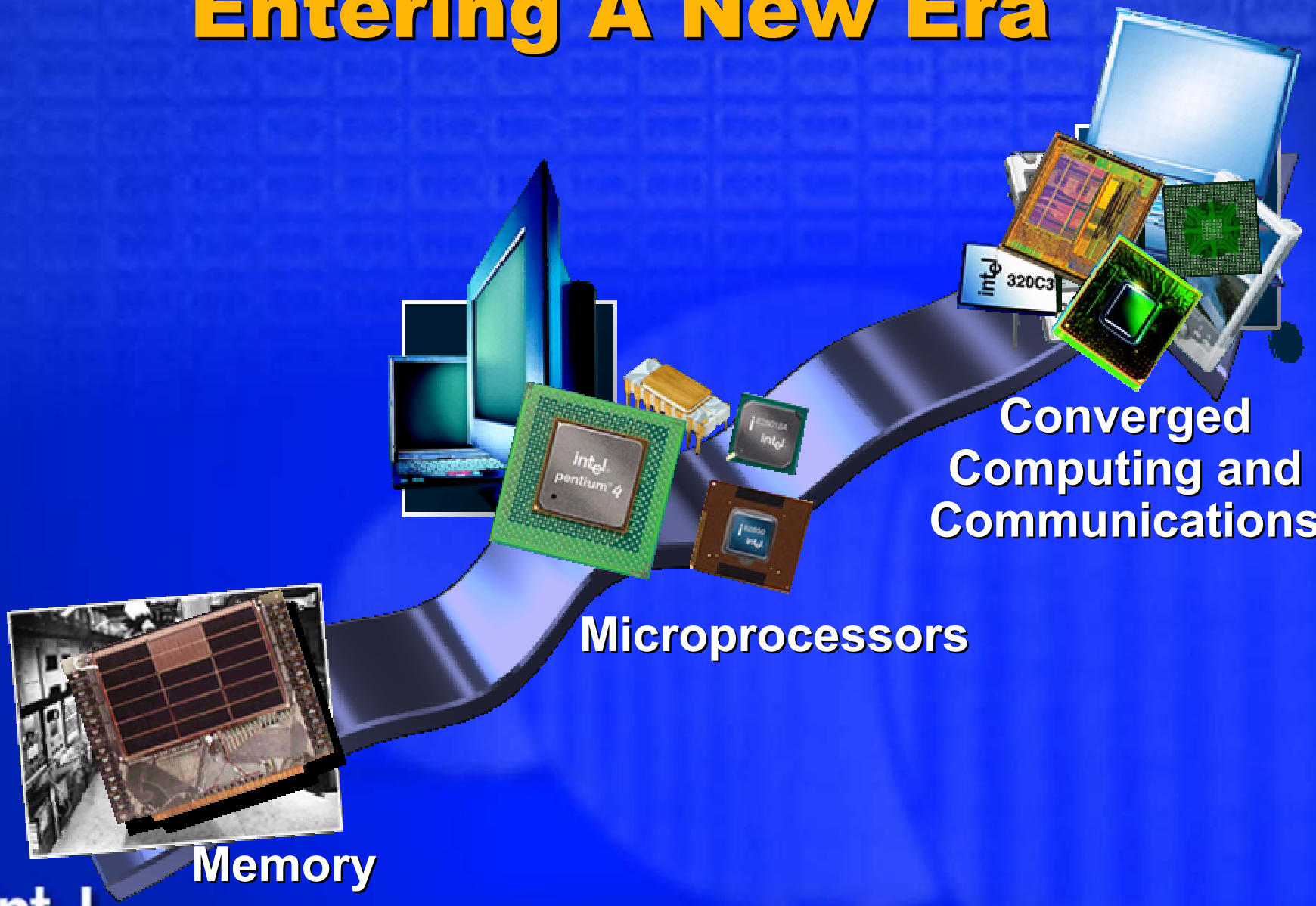
Agenda

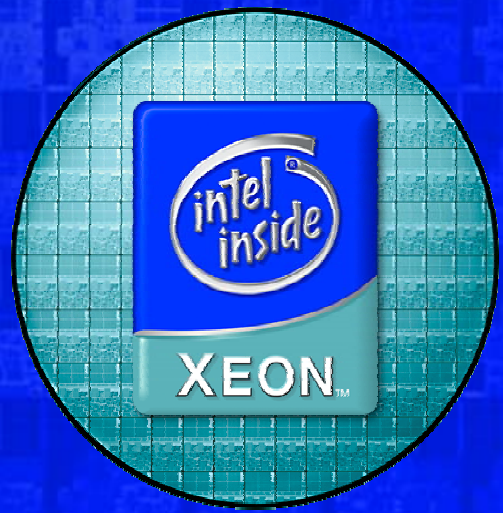
- Corporate Mission
  - Leadership in Technology
  - Leadership in Integration
- How do we continue to succeed?
  - Investments
  - Research and Development
  - Manufacturing Excellence
- Supplier Expectations
- Summary

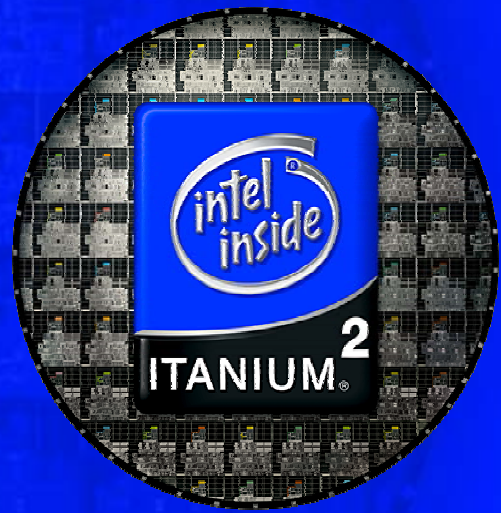
Entering A New Era



Leadership by Technology

Desktop





Server

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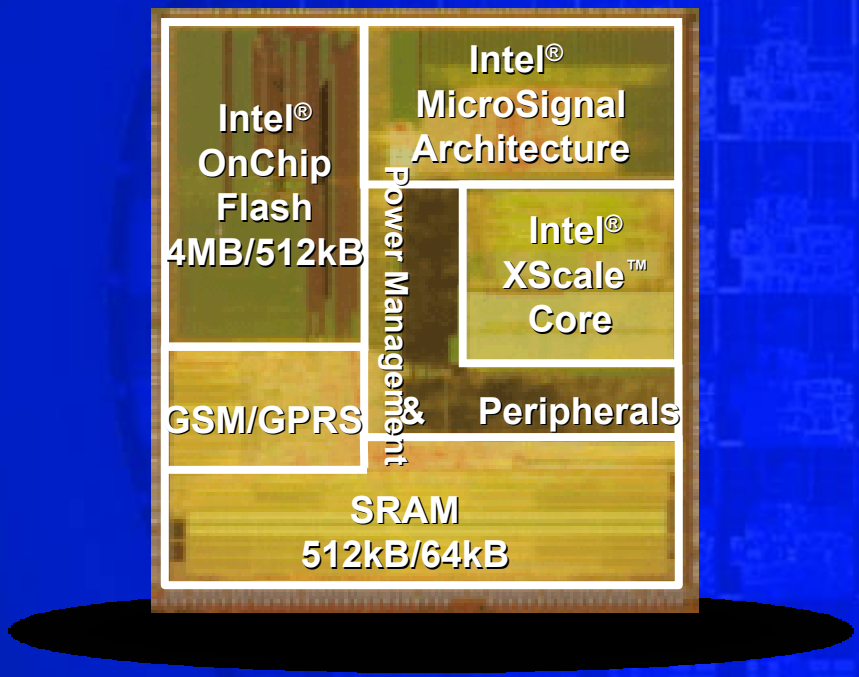
Leadership by Integration

Intel® PXA800F Processor

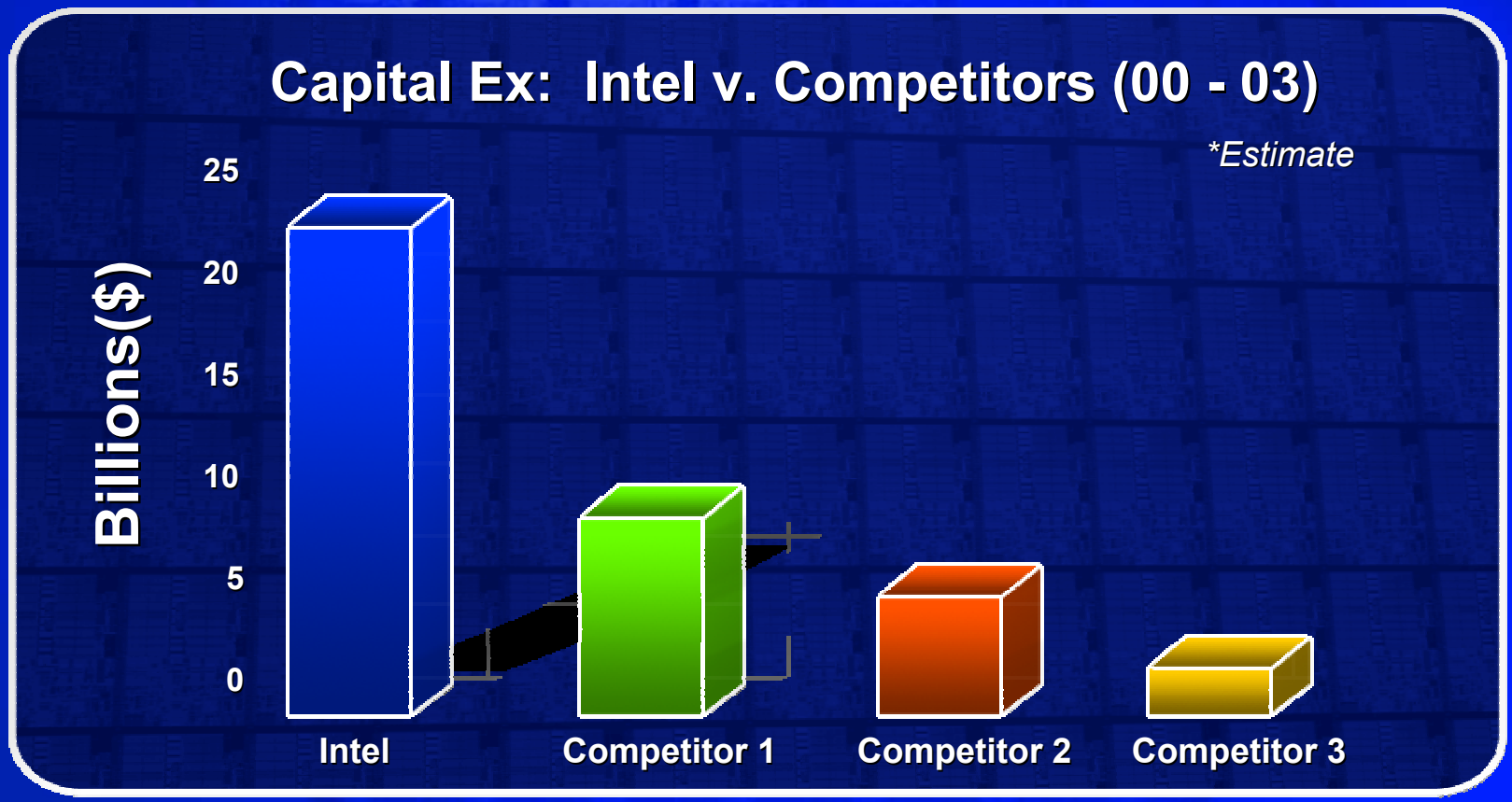


Intel® Mobile Technology

How do we continue to lead?

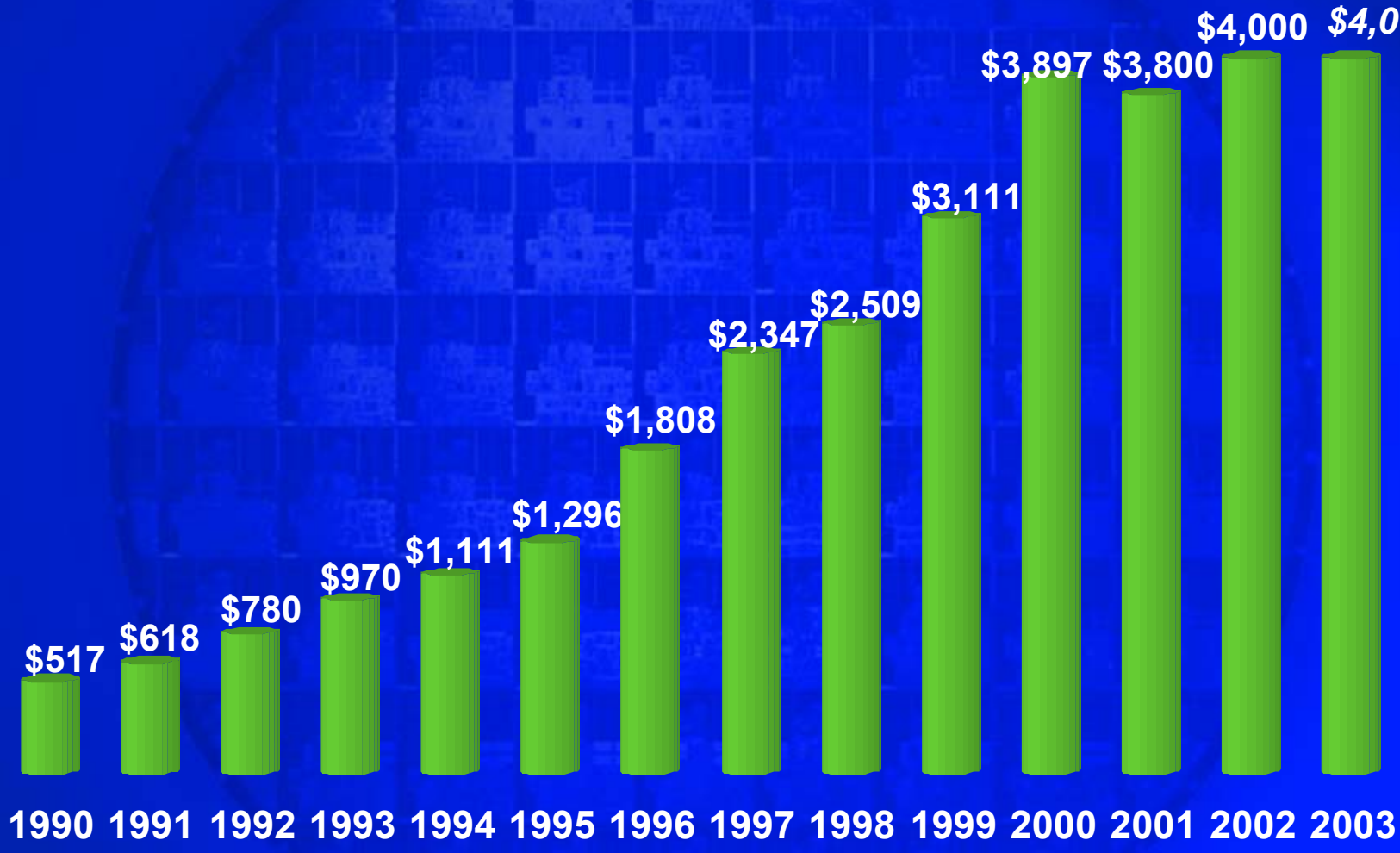
- Commitment through investments
- Commitment through advanced research and development – new technologies
- Continued, successful implementation of Moore's Law
- Commitment through manufacturing excellence

Intel Capital Expenses



Source: Intel

Intel R&D Investment ($M)



Source: Intel Annual Report

Worldwide Intel R&D Presence

75+ labs and over 7,000 R&D

Decentralized Approach Fosters Innovation

Technology Focus: Microprocessor Products

- Research Groups are de-centralized
  - Multiple sites
- Central Technology Development groups
  - Logic: Hillsboro, Oregon
  - Memory: Santa Clara, California
  - Packaging: Chandler, Arizona
- Copy Exactly! from Development into Manufacturing
  - Fastest and Highest Volume Manufacturing Ramp

Technology Focus: Logic

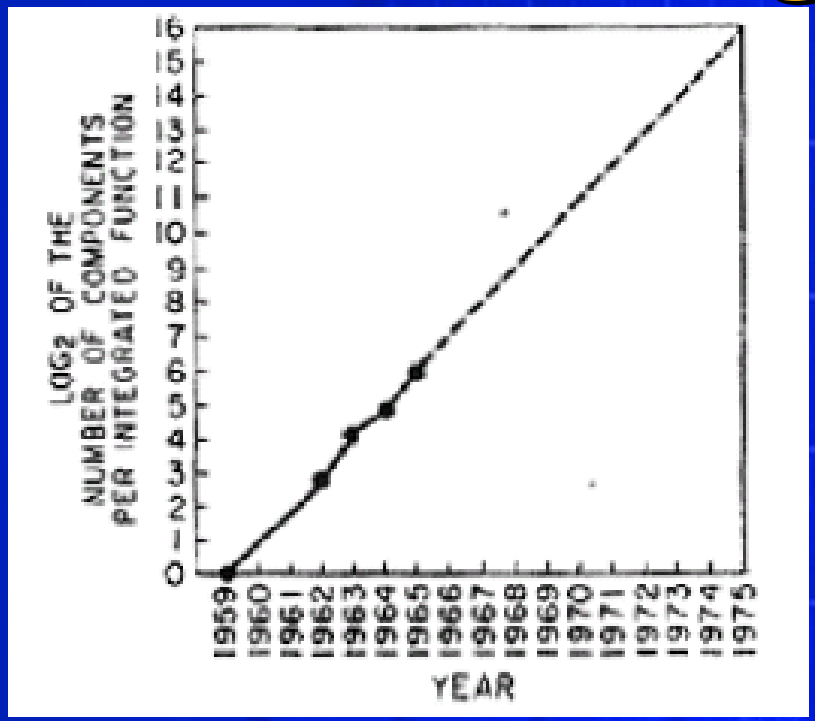
	Actual			Forecast			
Process Name	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1999	2001	2003	2005	2007	2009	2011
Lithography Node	180	130	90	65	45	32	22nm
Gate Length	130	70	50	30	20	15	10nm

Leadership through Technology

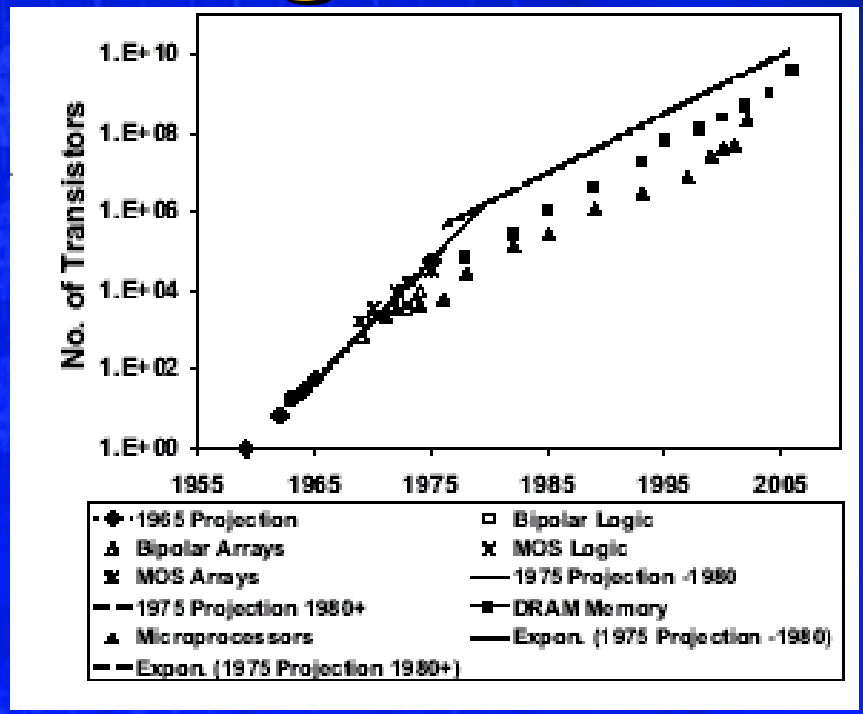
- Mission – to continue to provide leading edge technology in computing and communications
- Financial Challenges
- Technology Challenges
  - Increasing complexity
    - ...ive scaling
    - ...ew materials
    - added features (integrated capabilities)
    - New concerns: Power, heat

Moore's Law continues!

Moore's Law.... in the beginning

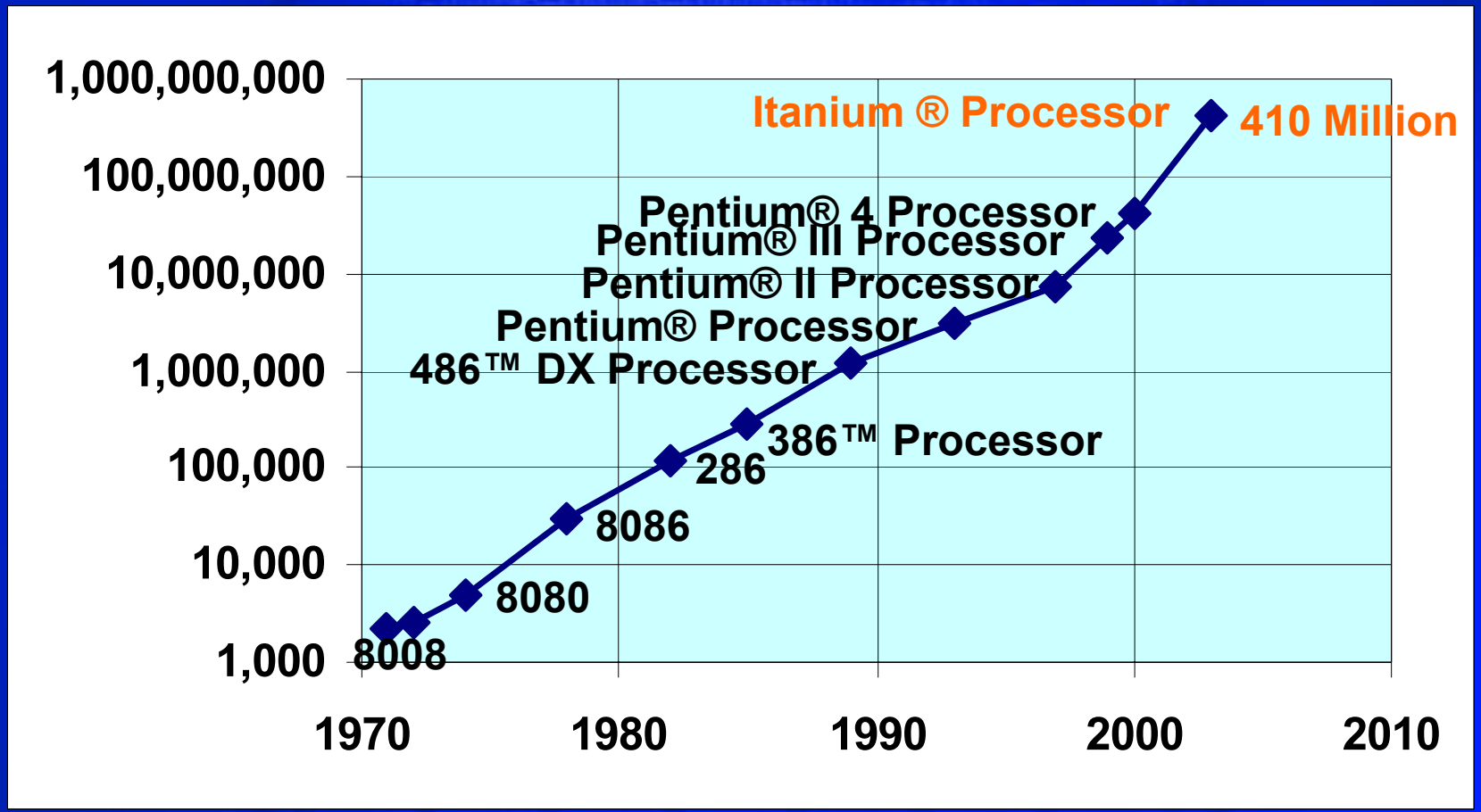


1965 Transistor Projection



1975 Transistor Projection

Moore's Law Today



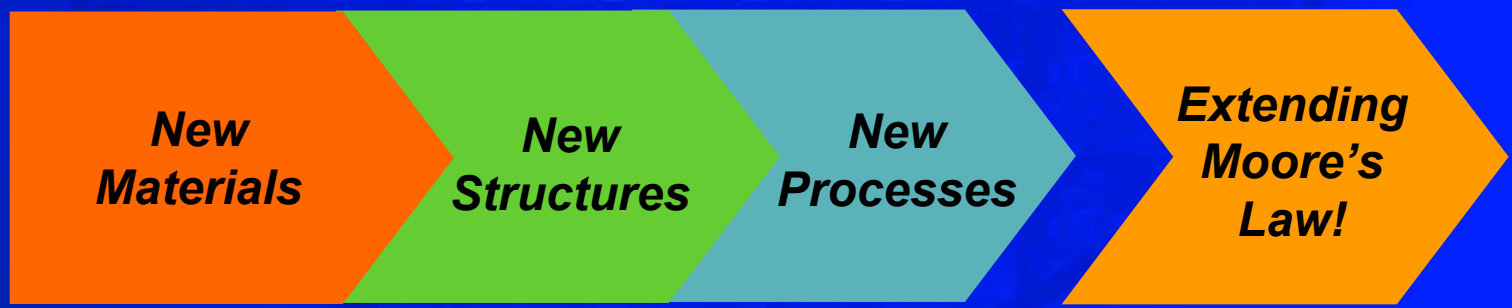
Heading toward 1 billion transistors in 2007

Moore's Law Economics
(Source: Intel, VLSIR)

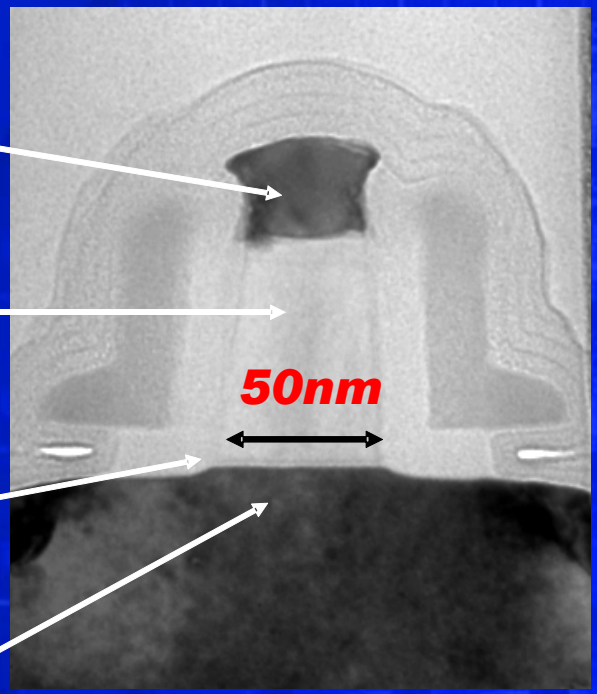
	1993	1998	2003
Wafer size, mm	200	200	300
Fab cost, $B	0.9	2	3
Fab capacity, kwpm	20	40	30 - 35 ~77 (200mm-equivalent)
$B/kwpm	0.04	0.05	0.04

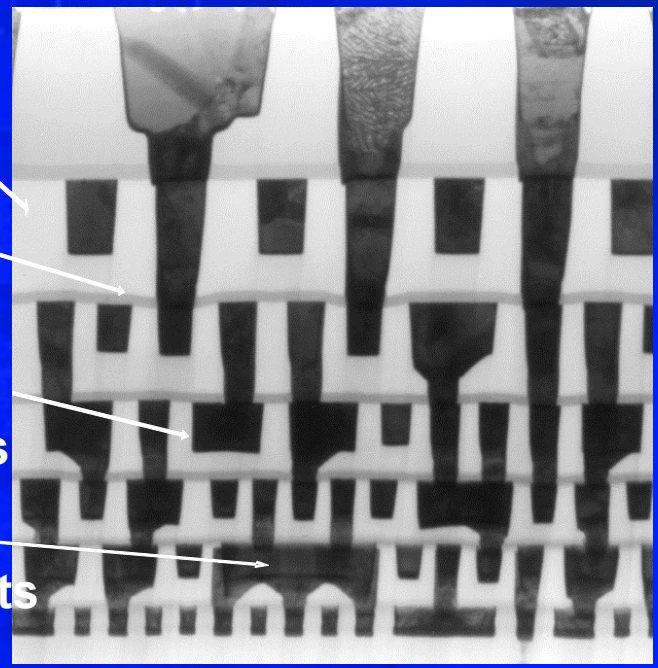
Evolution of Intel Process

	1997	1999	2001	2003	2005	2007	2009	2011
Node	0.25µm	0.18 µm	130nm	90nm	65nm	45nm	32nm	22nm
Litho	DUV	→	193nm	→	→	193/157	?	?
Metal	Al	→	Cu	→	→	→	→	?
ILD	SiO2	SiOF	→	SiOC	→	→	?	?
Gate Ox	SiO2	→	→	→	High-k?	?	?	?
Gate Electrode	Poly	→	→	→	→	Metal?	?	?



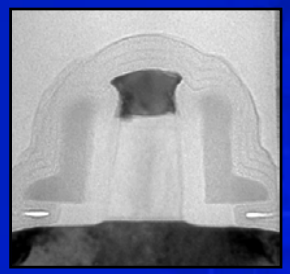
Success in 90nm development





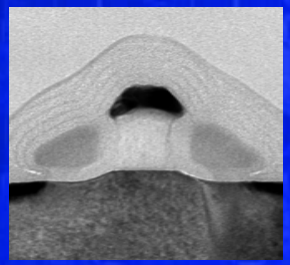
Driving Moore's Law Further

90nm Node
2003



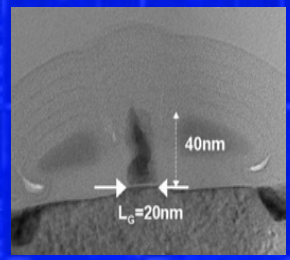
50nm Length
(IEDM2002)

65nm Node
2005



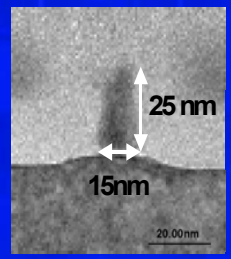
30nm Prototype
(IEDM2000)

45nm Node
2007



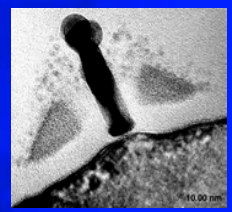
20nm Prototype
(VLSI2001)

32nm Node
2009



15nm Prototype
(IEDM2001)

22nm Node
2011



10nm Prototype
(ITJ 2002)

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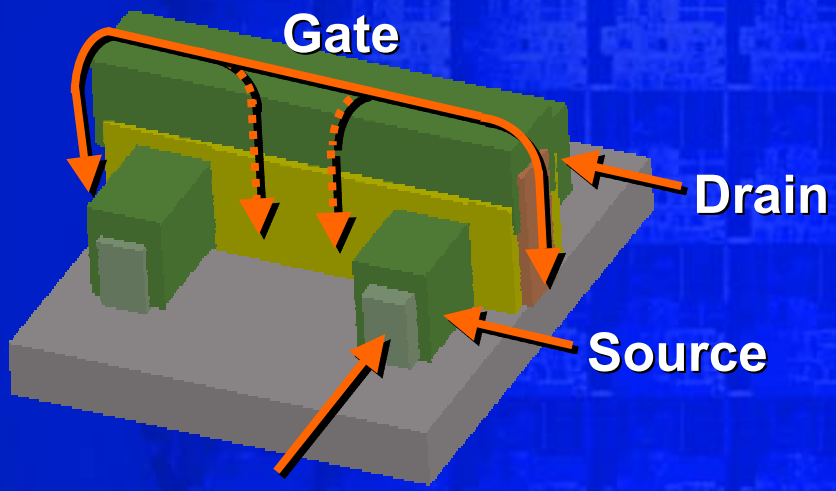
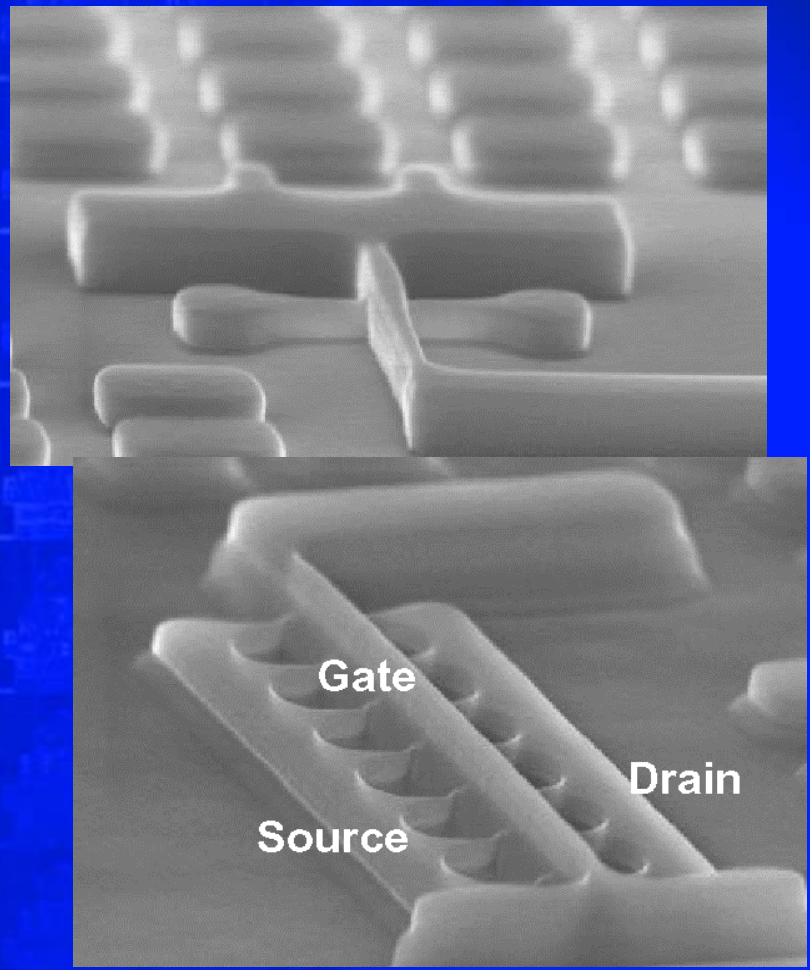
Working on Advanced Transistor Architecture
➔ New Process➔ Need New Materials





World record breaking NMOS performance demonstrated today!

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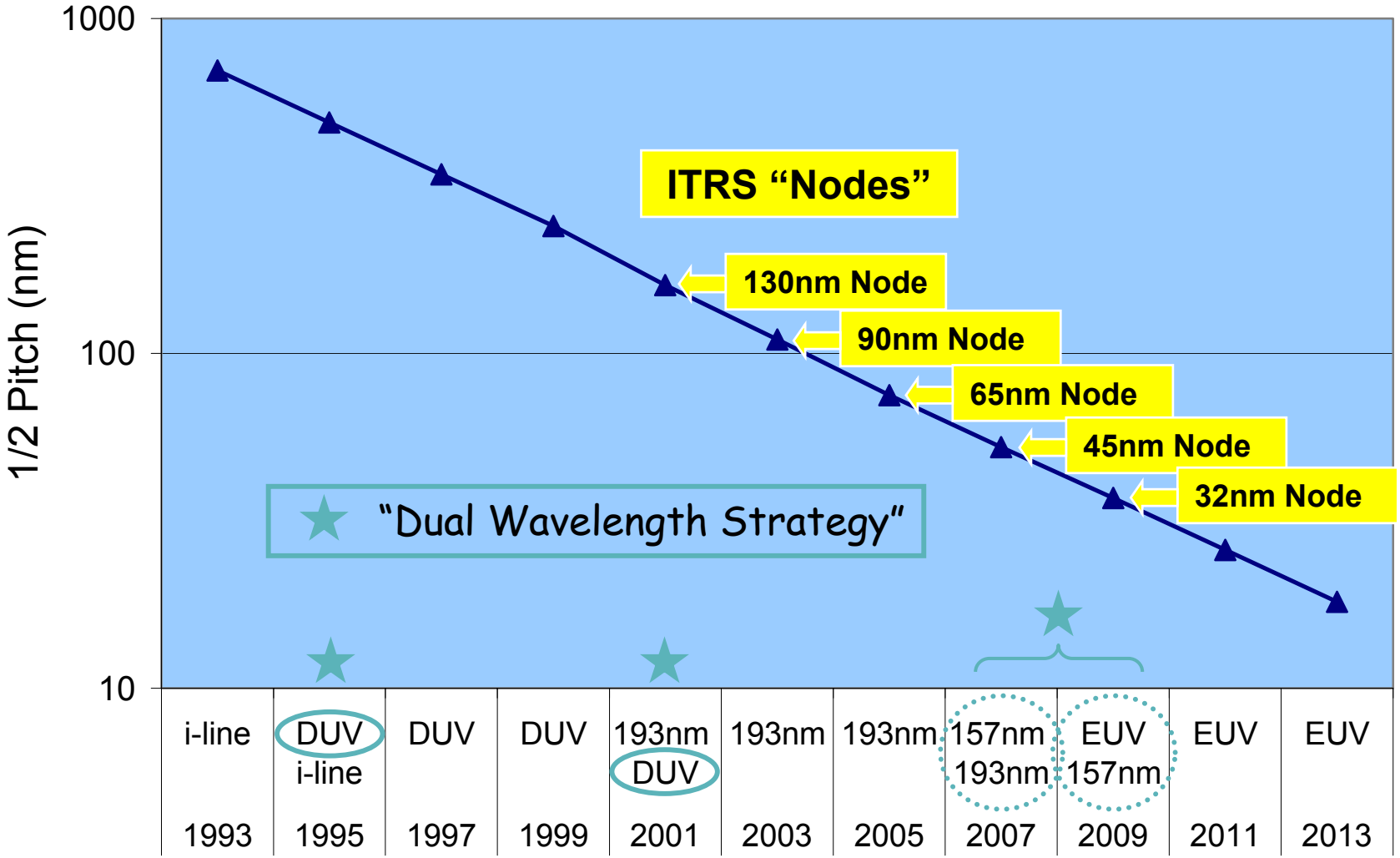
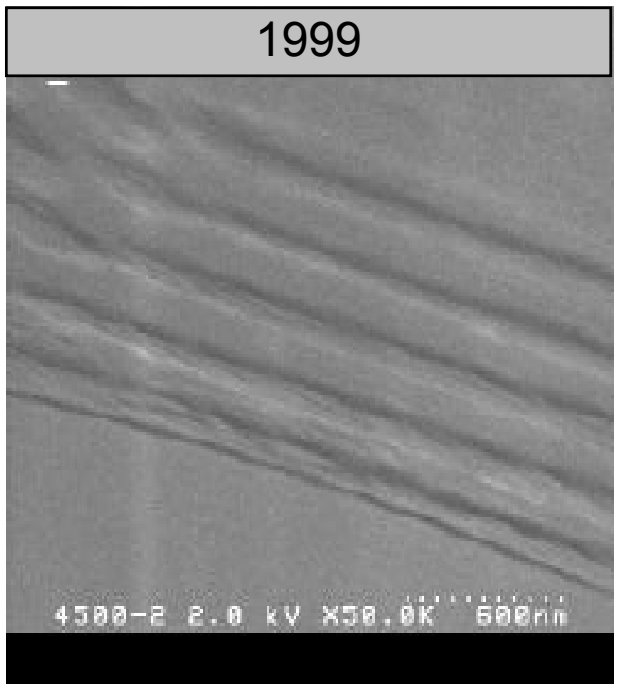
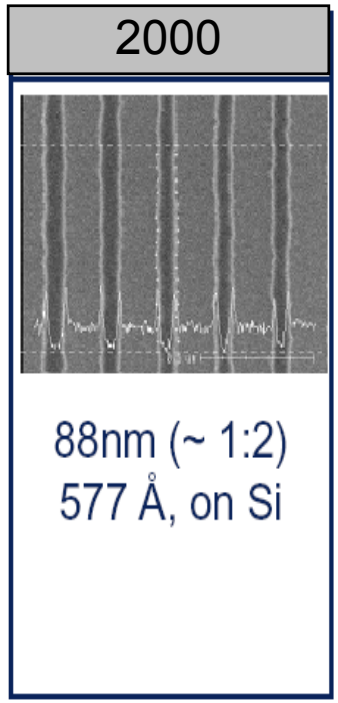
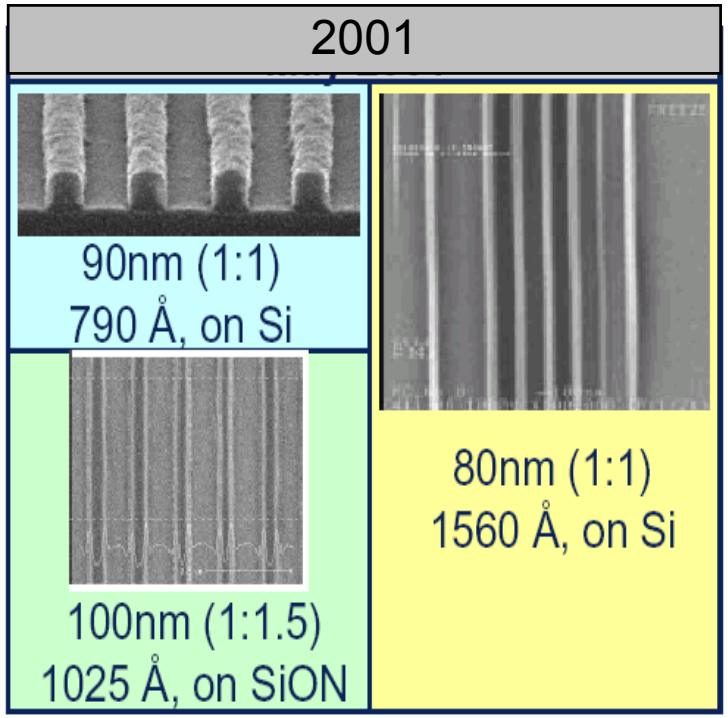
Intel Lithography Roadmap



157nm Lithography







157nm lithography is maturing:

- Research tools shipping in 2003
- Development tools scheduled for 2004
- Single layer resists are making rapid progress

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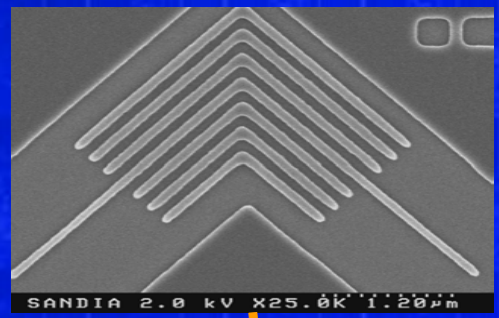
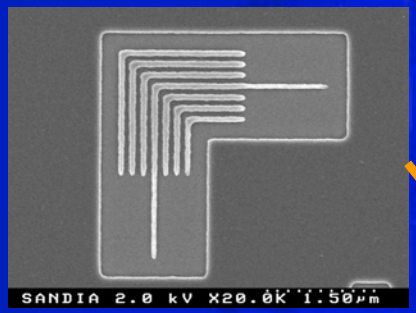
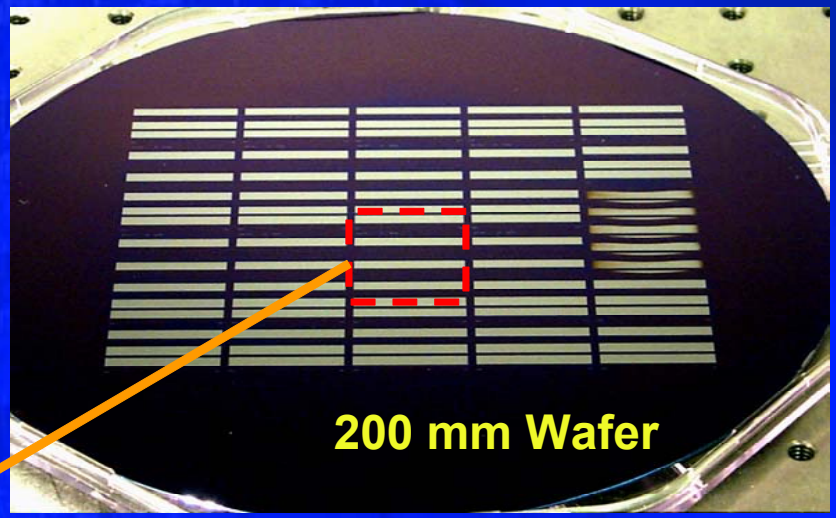
EUV Lithography - Full Field ETS images
(using 0.1 NA system)

100 nm Elbows 1:1



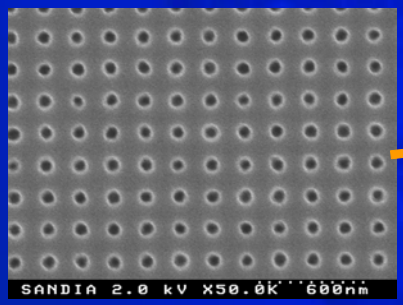
80 nm Elbows 1:1

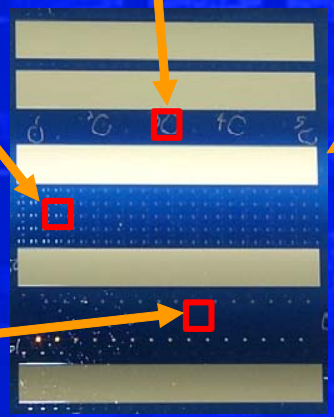




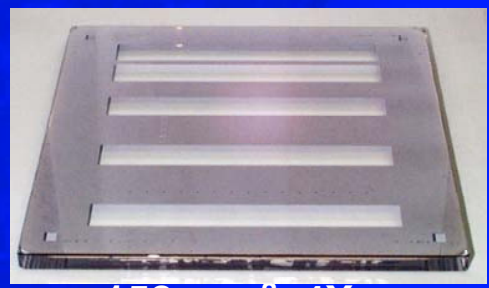
4x5 matrix

100 nm contacts 1:1





24 x 32.5 mm^2 field



152 mm^2, 4X
Reflective Mask

Printing 80 nm images at 0.1 NA is equivalent
to printing 32 nm with 0.25 NA production system

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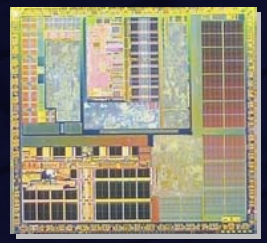
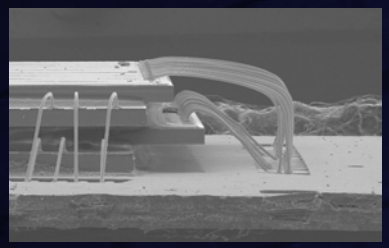
Leadership By Integration

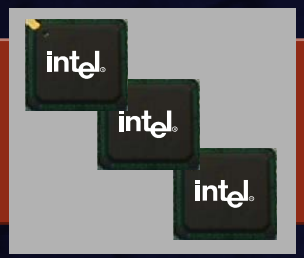
Computing + Communications on One Chip



Silicon Level Integration
Functions combined on single chip



Package Level Integration
Stacked discrete chips and packages



Functions on Discrete Chips
Flash, Applications processors, Cellular chipsets

2002 2004 2006

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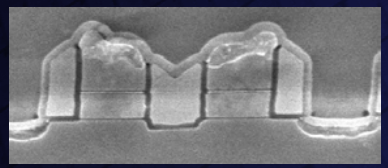
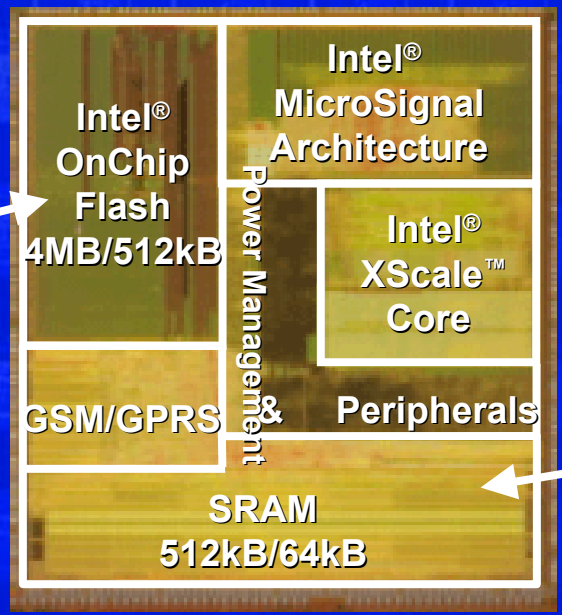
Wireless Internet on a Chip by Flash+Logic Integration

Intel® PXA800F Processor

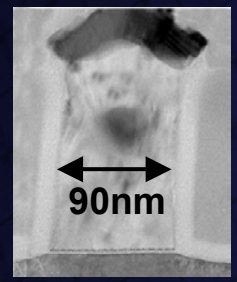
Flash



0.16µm² Flash Cell



Logic

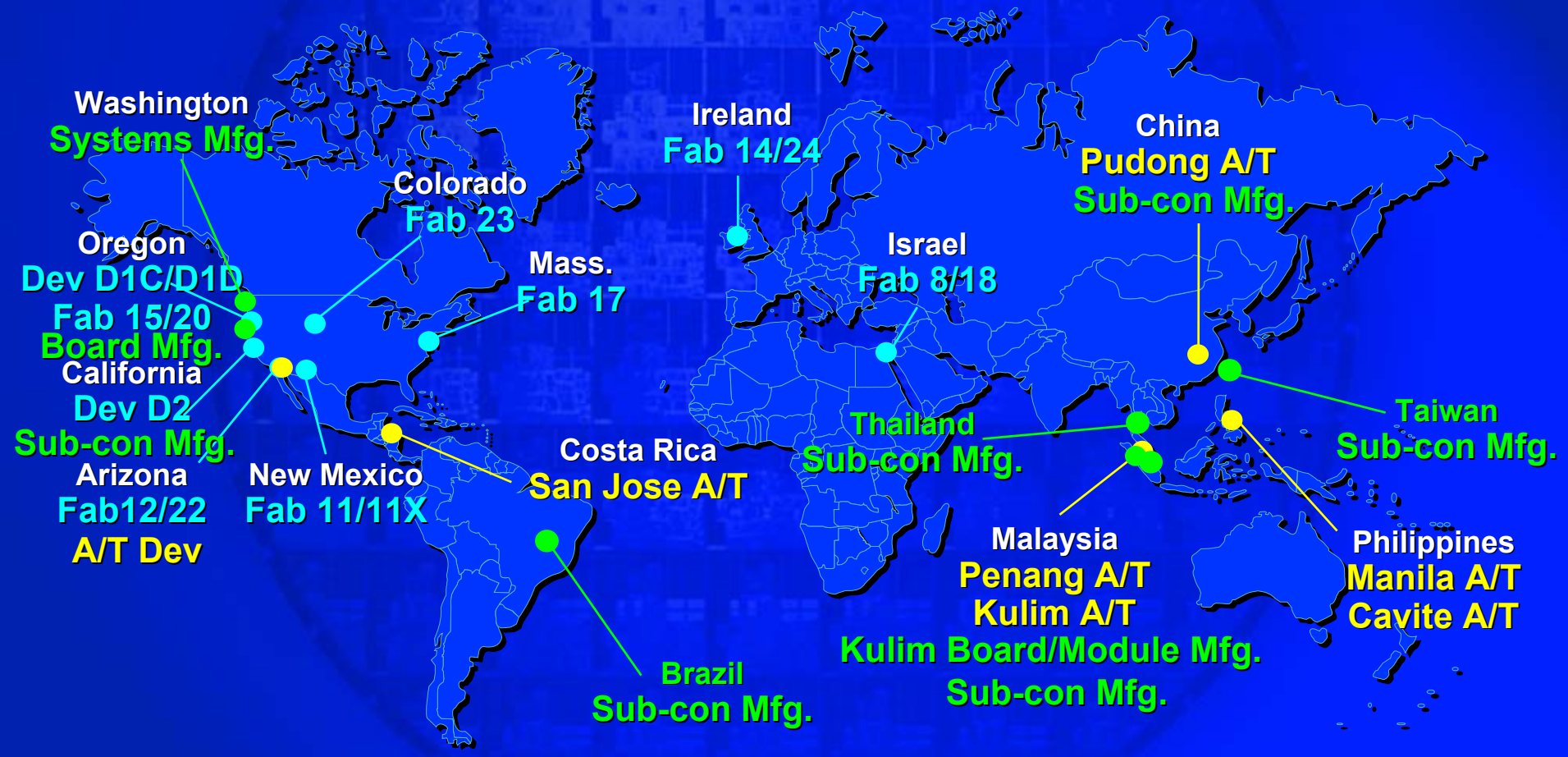


90nm Transistor Gate

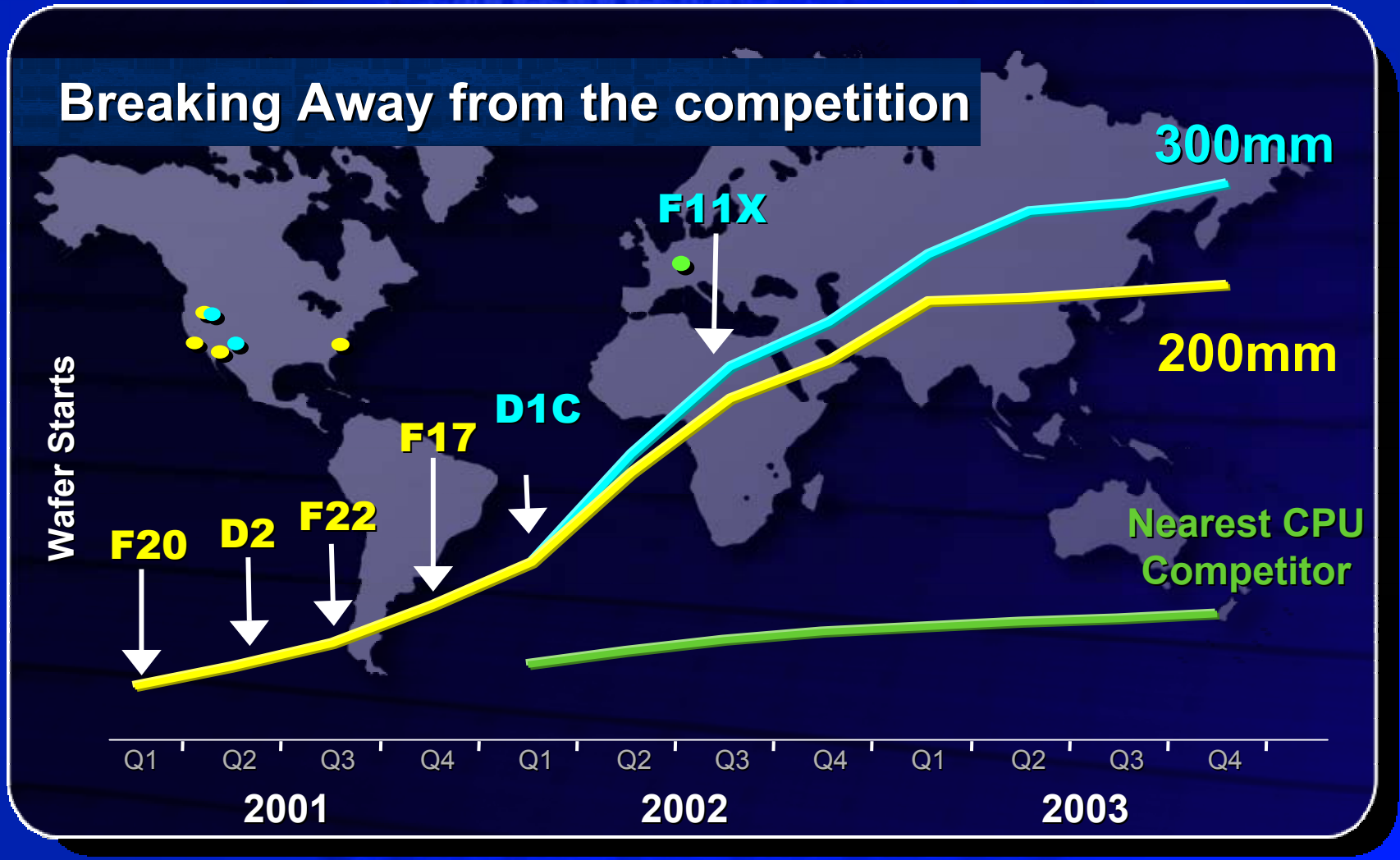
Continued Manufacturing Excellence

- 0.13 μm manufacturing leadership
- Worldwide Presence
- Intel Manufacturing Philosophy
  - Technology Development and Manufacturing Linked
  - Copy Exact! Transfer of Processes
  - Manufacturing Efficiency → 300mm Production
  - Leading Edge Capacity

Intel's High Volume Manufacturing Sites



0.13µm(130nm) Leadership

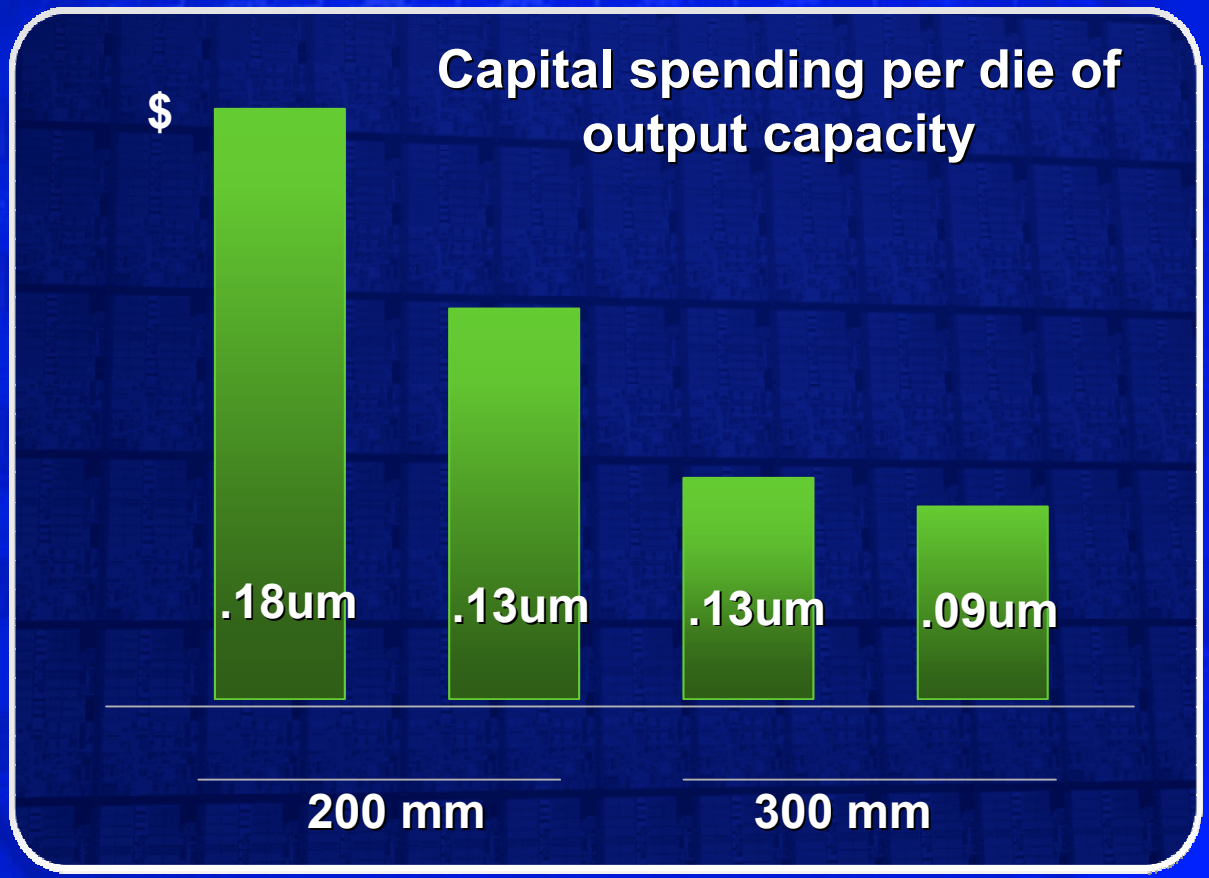


Source: Intel

Logic Development:
Linking 300mm Research, Development, and Production

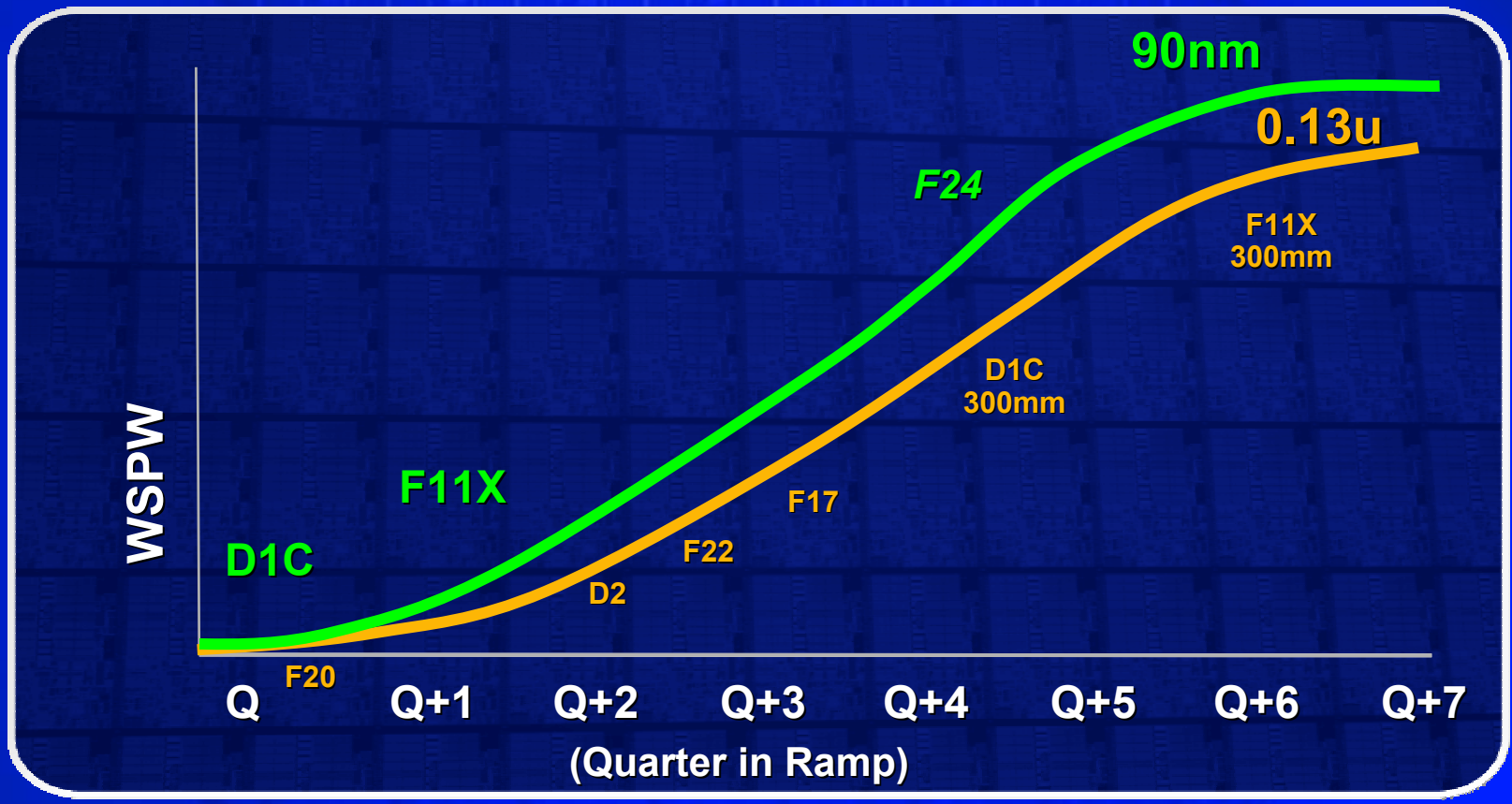
Source: Intel

Manufacturing Efficiency



Source: Intel

Scale: Leading Edge Capacity



**Source: Intel Estimates

Supplier Expectations

- Manufacturing excellence
  - Timely, cost-efficient support during HVM ramp
  - Quality systems
- Advanced Development
  - New equipment and capabilities matched with Intel's roadmap
  - Process Development
- Research
  - Collaborative efforts to foster innovation

Summary

Intel is committed to the future technologies

Success starts with the present

- 90nm technology innovation
- 90nm ramp in 2H'03

...and leads to the future

- continued extension of Moore's Law
- Package level integration
- System on a chip

For further information on Intel's silicon technology and Moore's Law, please visit the Silicon Showcase at www.intel.com/research/silicon